#5/Election
6-13-02
R. Hasha

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PATENT APPLICATION

Application
Inventor(s): Krivokapic et al.
SC/Serial No.: 09/711,445
Filed: November 13, 2000
Title: SELF ALIGNED TRIPLE GATE SILICON-ON-INSULATOR (SOI) DEVICE

Art Unit: 2811
Examiner: Owens, Douglas W.

Customer No. 23910

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited in the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, Washington, DC 20231, on May 15, 2002.

(Attorney Signature)

Stephen R. Bachmann, Reg. No. 50,806
Signature Date: May 15, 2002

RESPONSE A TO OFFICE ACTION UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, DC 20231

Sir:

This RESPONSE A is in reply to the Office action mailed April 19, 2002.

The Examiner has indicated that restriction to one of two groups is required under 35 U.S.C. 121. Group 1 includes claims 1-12, which are drawn to a transistor and classified in class 257, subclass 397. Group 2 includes claims 13-21, which are drawn to a method of making a transistor and classified in class 438, subclass 297+.

Applicant hereby elects Group 2, claims 13-21, to be examined in the present application. Applicant believes this election does not require an amendment to the inventorship of the present application.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 06-1325 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: 5/15/02

By: _____
Stephen R. Bachmann
Reg. No. 50,806

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